3D Printed Microelectronics & New Design Thinking

Applications Engineering

Oct 5th, 2022

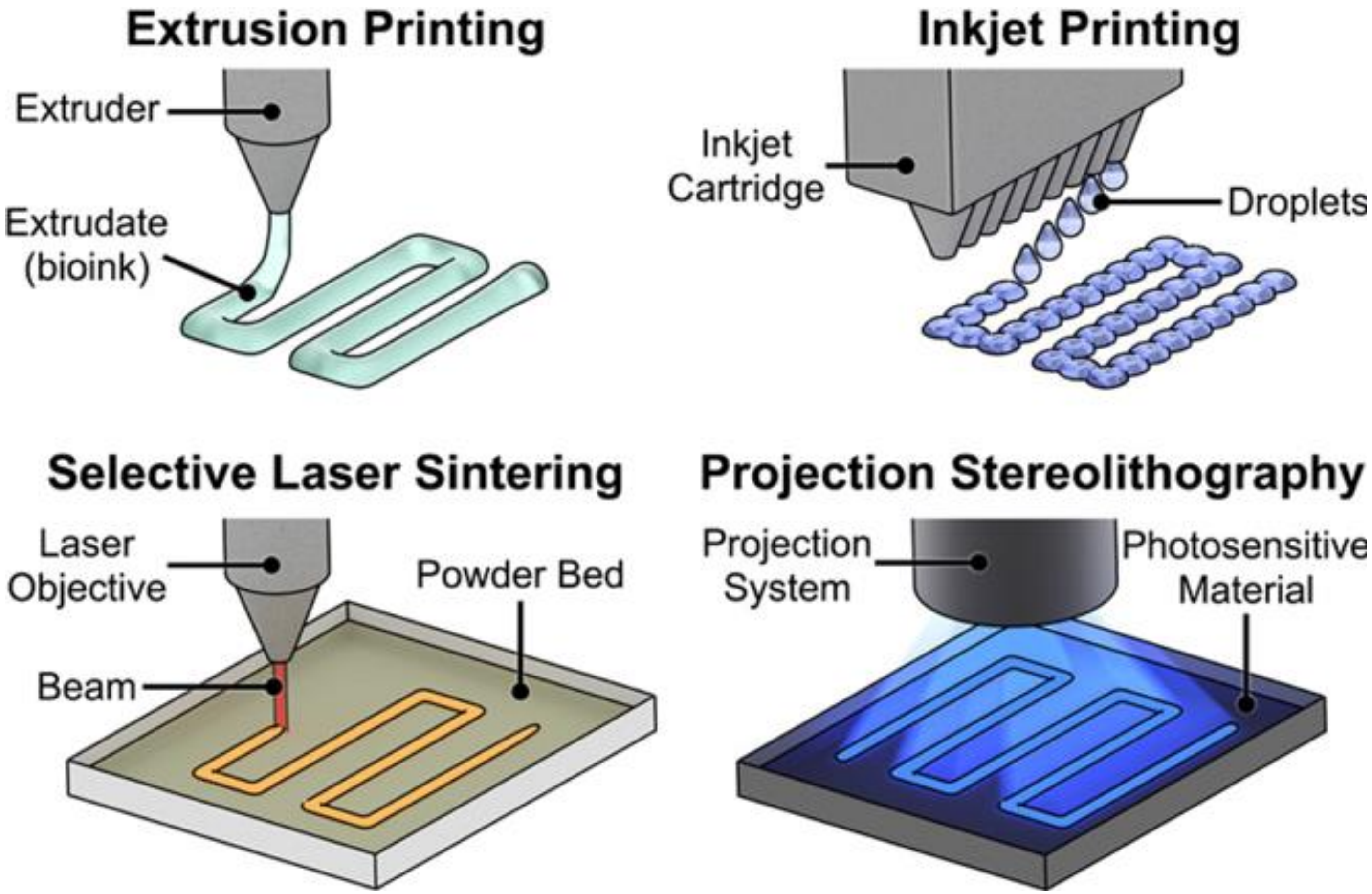
Agenda

- Introduction
- AME process – Generalities
- AME potential – New Design Thinking
    - 3D space area reduction
    - Sockets & Interposers
    - Embedding & encapsulation
    - Non-planar transmission lines
    - Electromechanical
- Going from 2D to 3D ECAD

Additive Manufacturing (3D printing) - Generalities

- AME 3D Printing is a process for making a **physical object** from a digital model, by laying down many successive thin layers of a material.

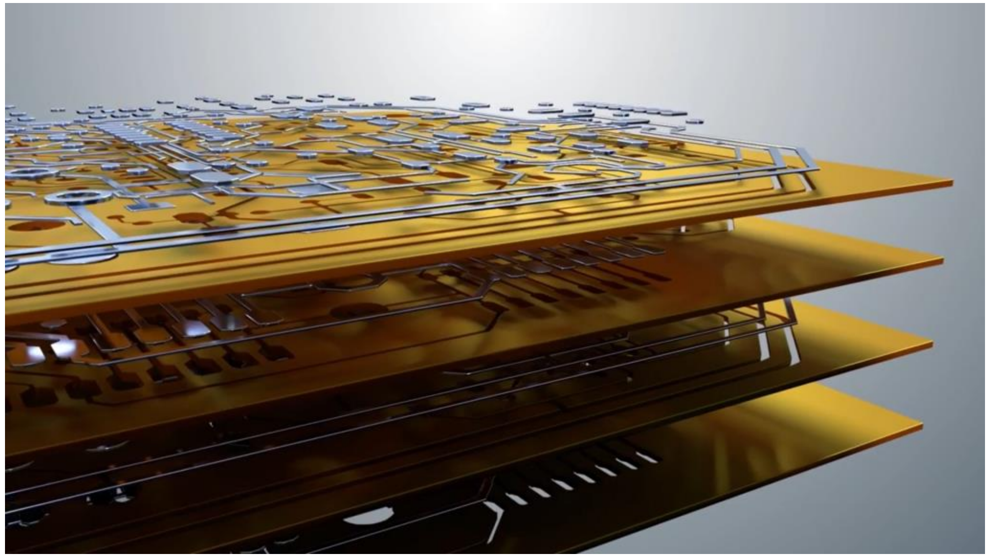
- Types of 3D printing processes:
  - Stereolithography
  - Extrusion
  - SLS
  - INKJET

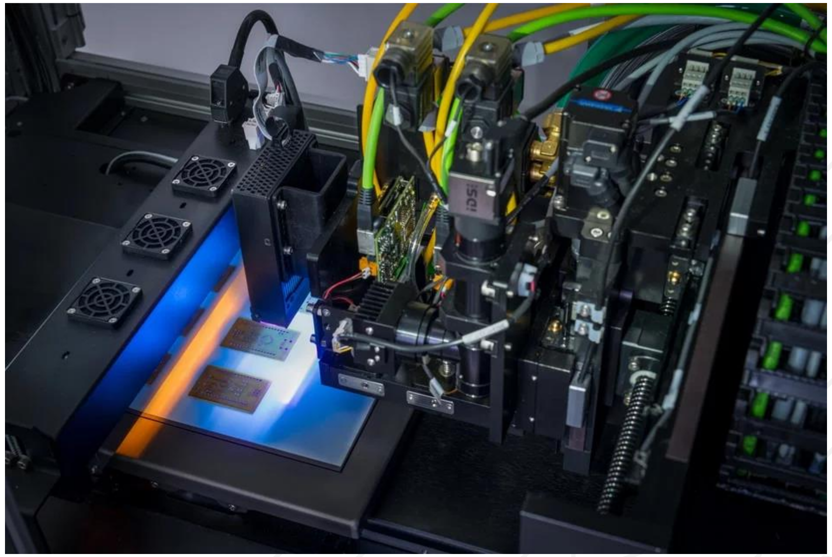


Additive Manufacturing Electronics (AME)

NANODIMENSION PROCESS DESCRIPTION

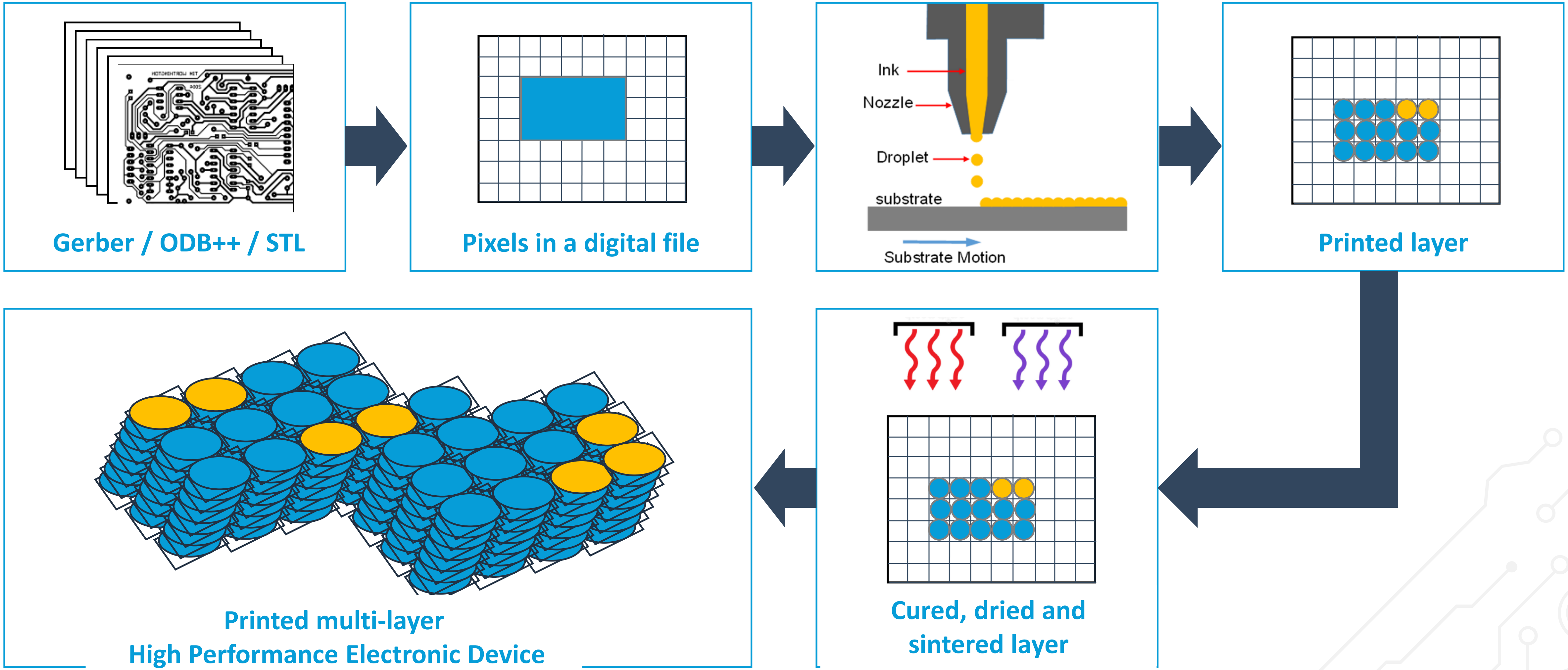
- Inkjet technology that combines UV-cured dielectric material (acrylic monomers) with silver nanoparticles (Ag NP) that undergo sintering upon IR radiation.
  - Result in solid objects with highly conductive patterns in shapes unachievable through traditional processes





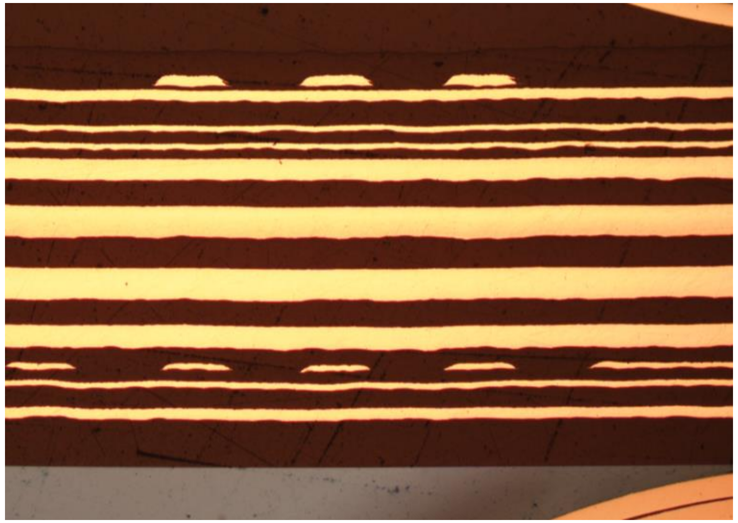
Additive Manufacturing Electronics (AME) - DragonFly

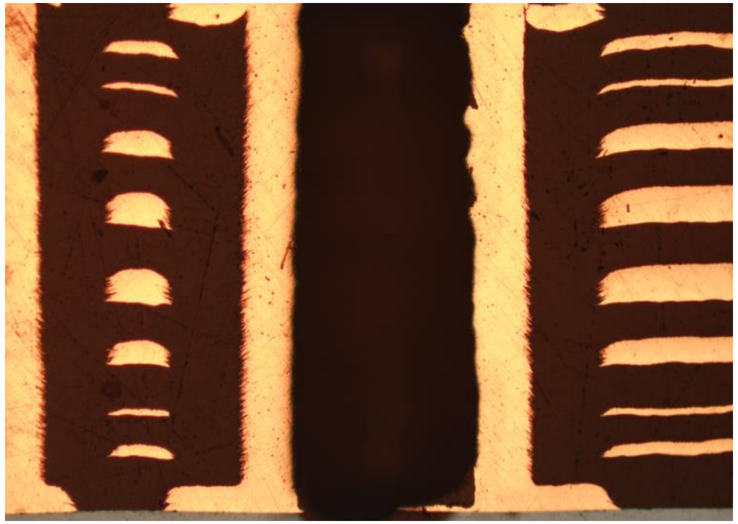
From a Digital design file to a Printed Hi-PED

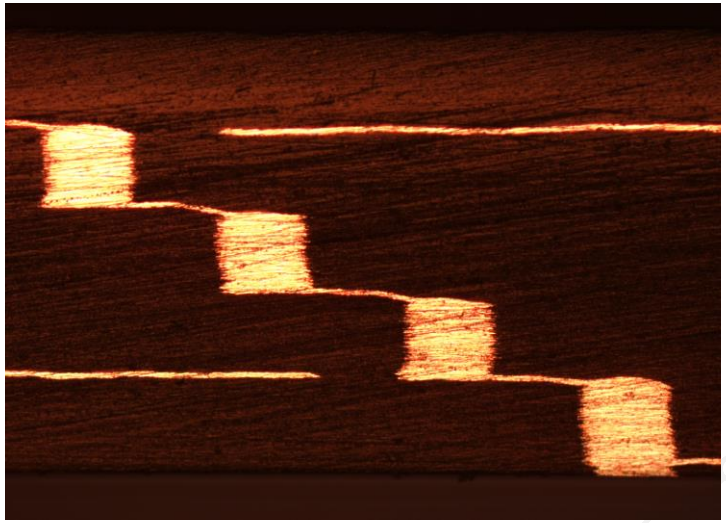


AME BUILD

CROSS-SECTIONAL VIEW



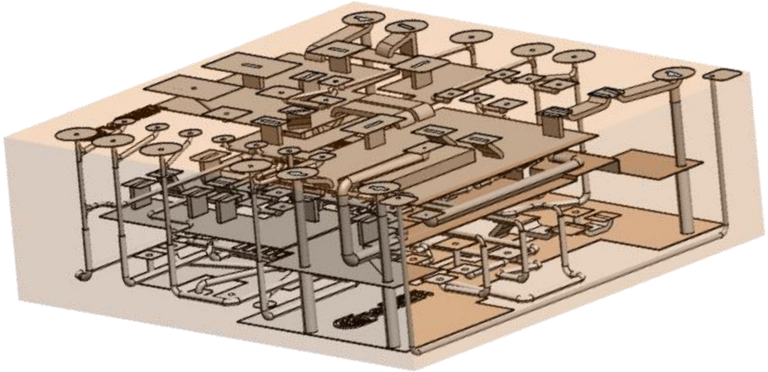


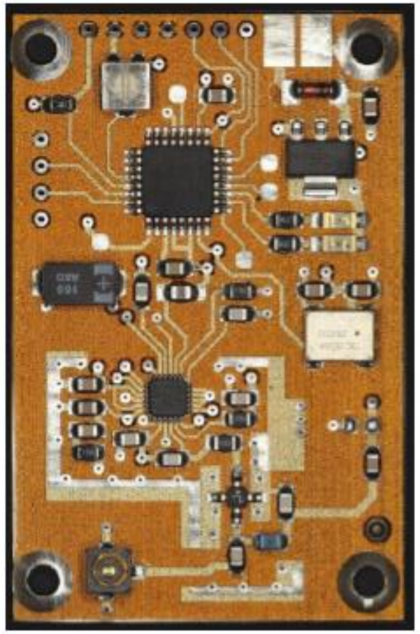


New Design Thinking

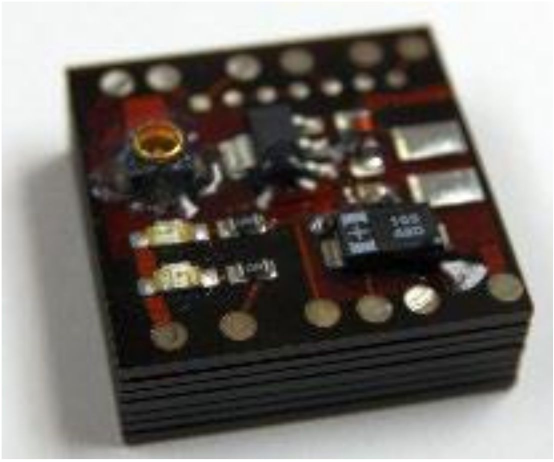
AREA REDUCTION BY 3D SPACE USAGE

- Stack of a splitted design in “Z” by creating component cavities

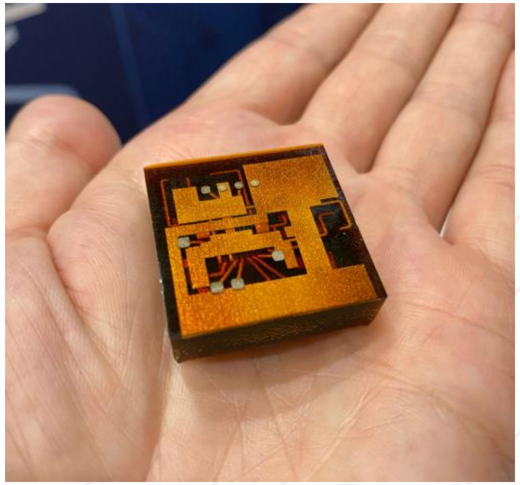




PLL board



PLL Cube (stacked)

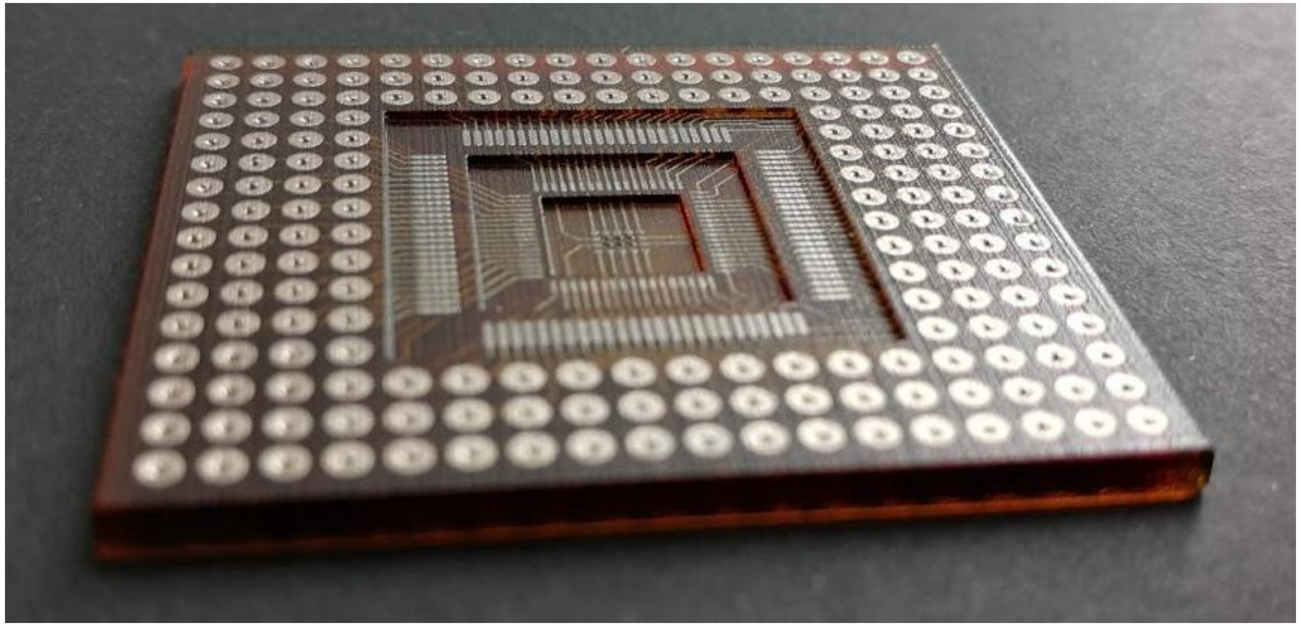


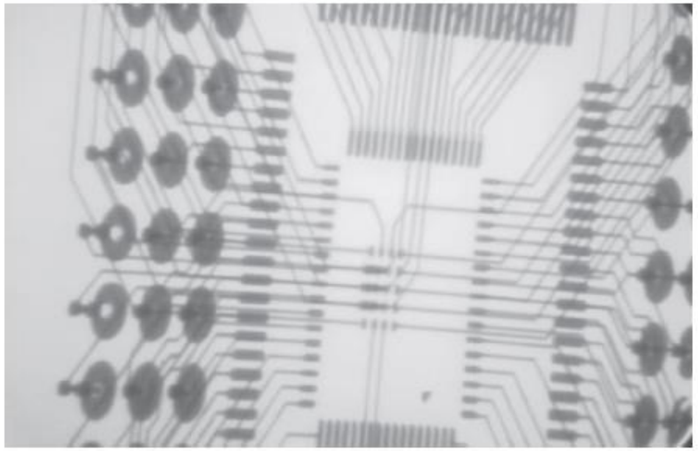
PLL Cube (embedded)

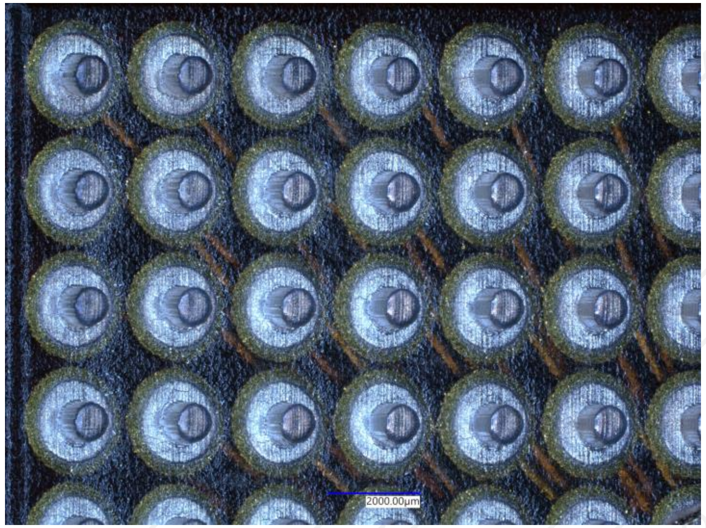
New Design Thinking

SOCKETS & INTERPOSERS

- Low-resistance Mechanical shapes can be 3D printed on-site, rather than more complex processes.





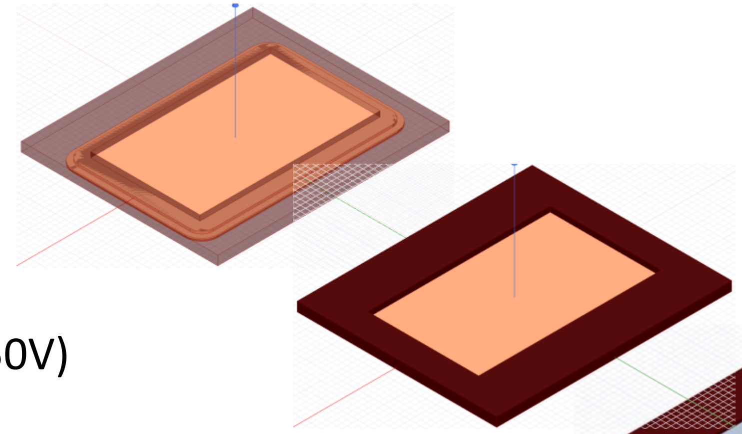


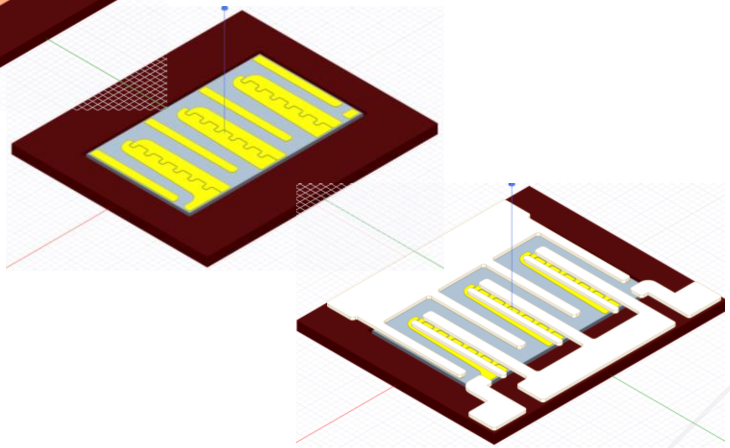
Source: J.A.M.E.S

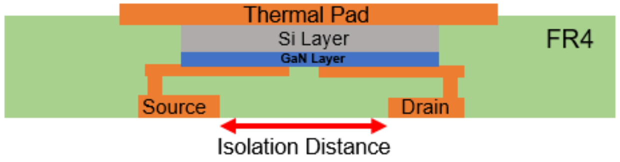
New Design Thinking

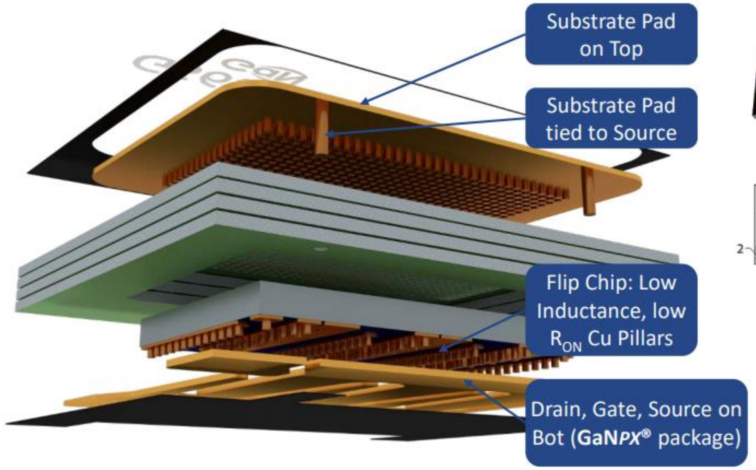
EMBEDDING & ENCAPSULATION

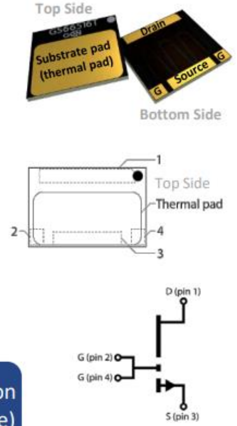
- Enhancement mode GaN-on-silicon power transistor (650V)
- Top-side cooled configuration
- High current $\mathrm{Ids}(max) = 60A$
- $\mathrm{Rds}(on) = 25m\Omega$
- Very high switching frequency (> 100MHz)
- Small 9 X 7.6 mm PCB footprint

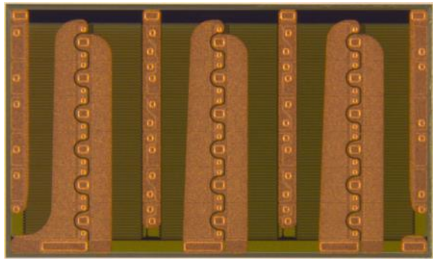


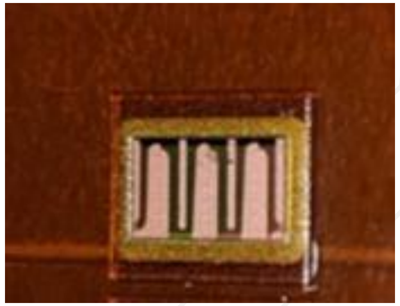


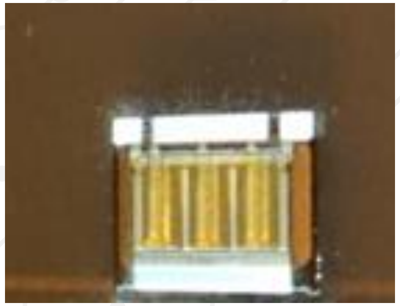






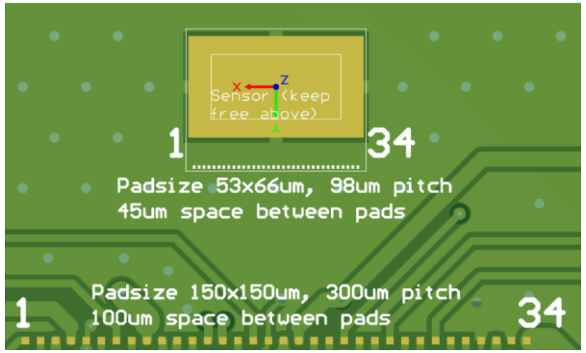


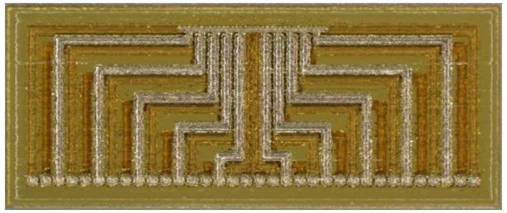


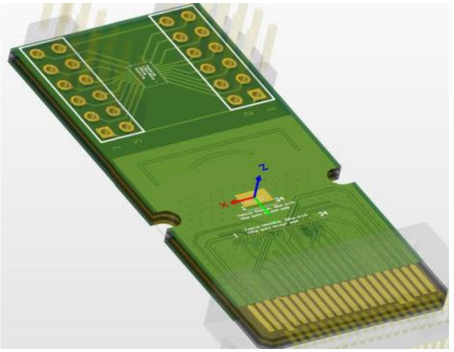


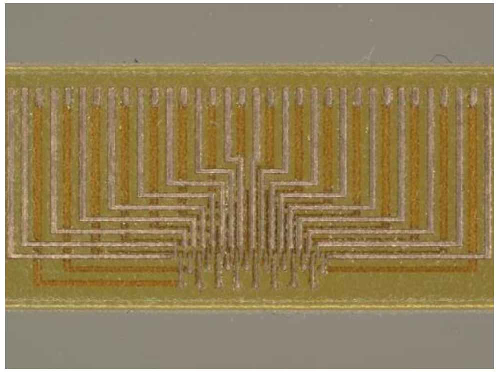
New Design Thinking

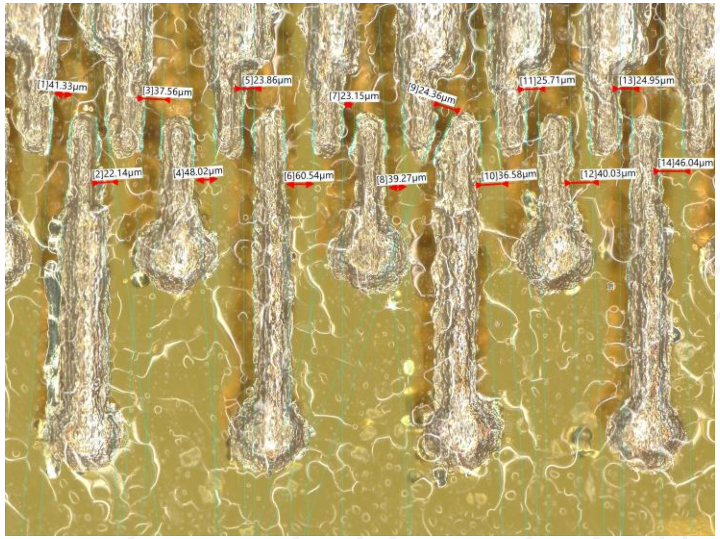
EMBEDDING & ENCAPSULATION - MIMIC WIRE BONDING







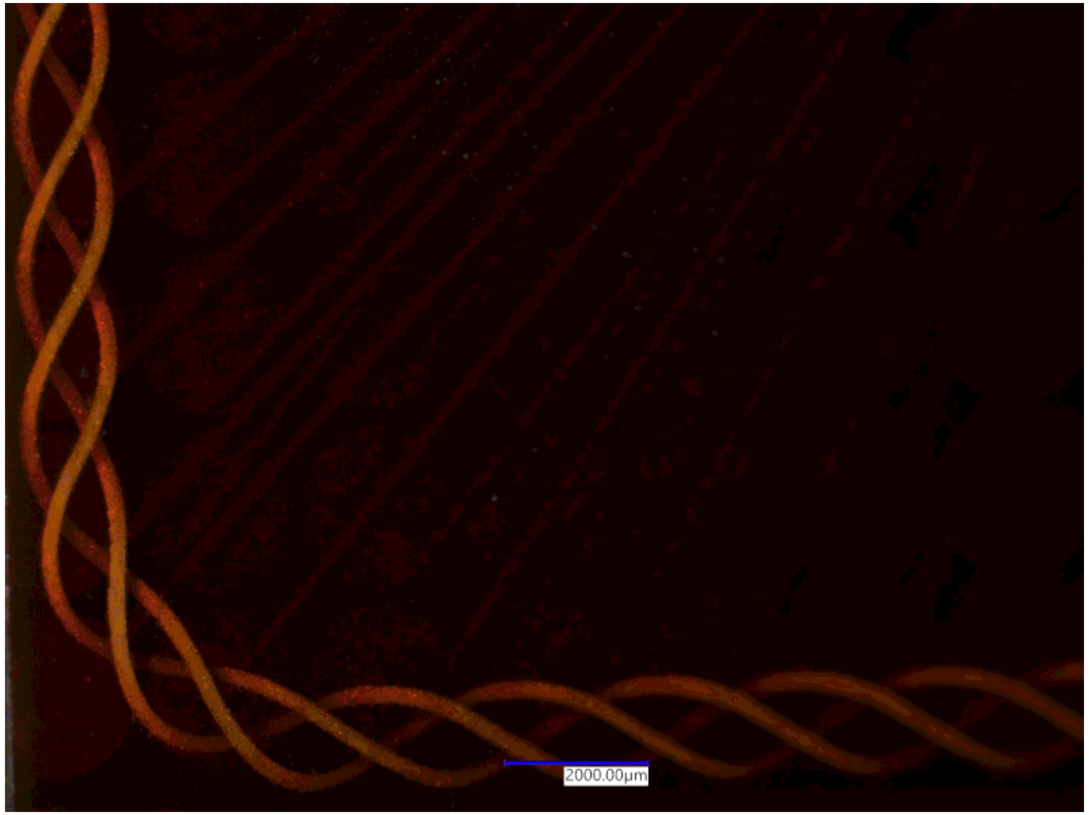




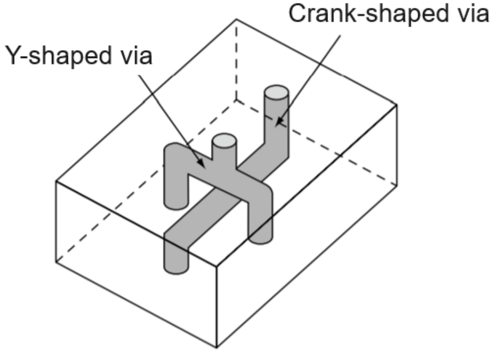
New Design Thinking

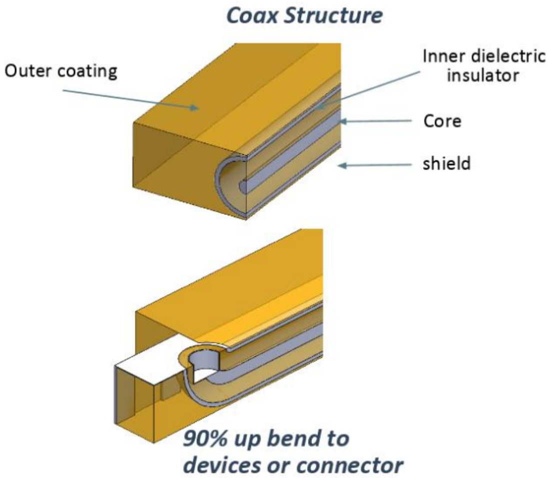
NOISE AVOIDANCE & NON PLANAR TRANSMISSION LINES

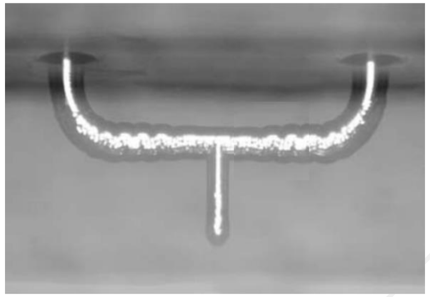
- Coaxials, twisted pairs, waveguides. Freedom of via interconnects

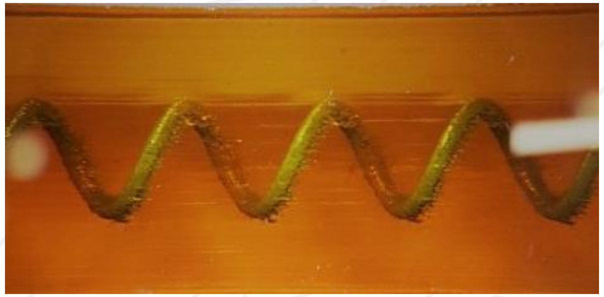


Source: J.A.M.E.S







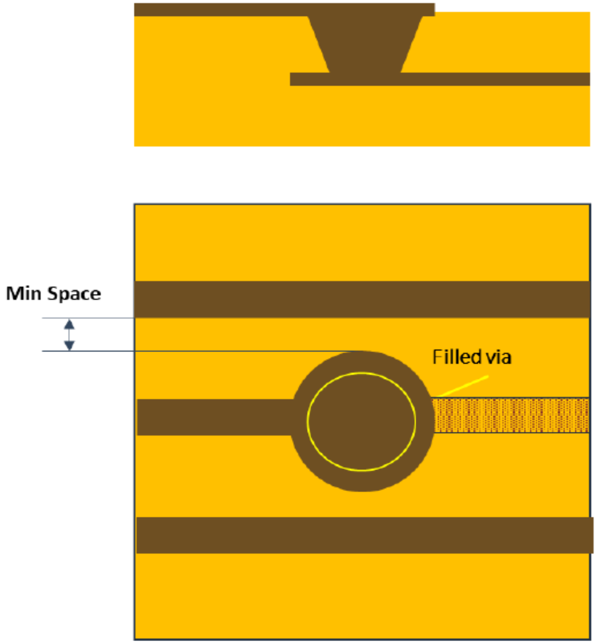


New Design Thinking

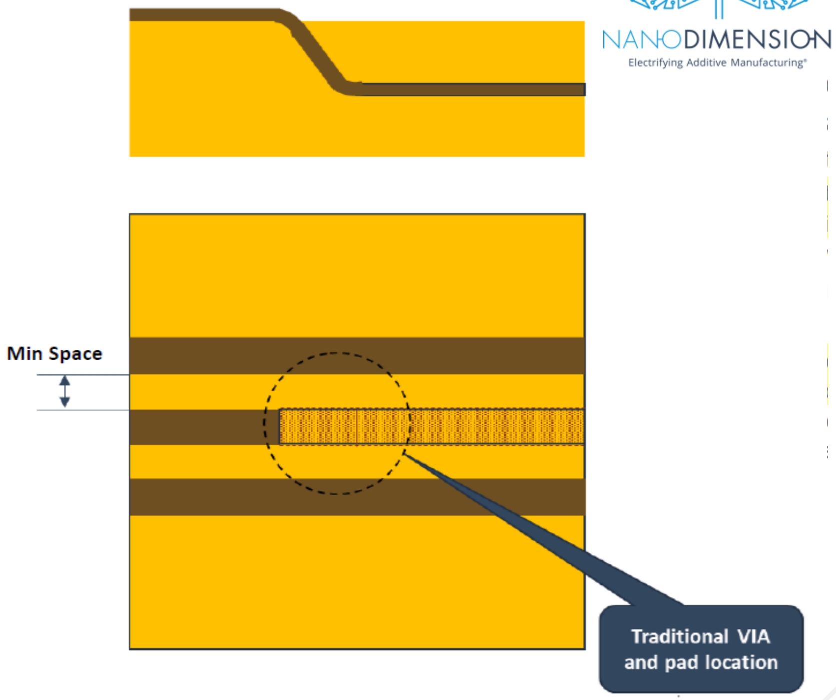
HIGHER DENSITY ROUTING

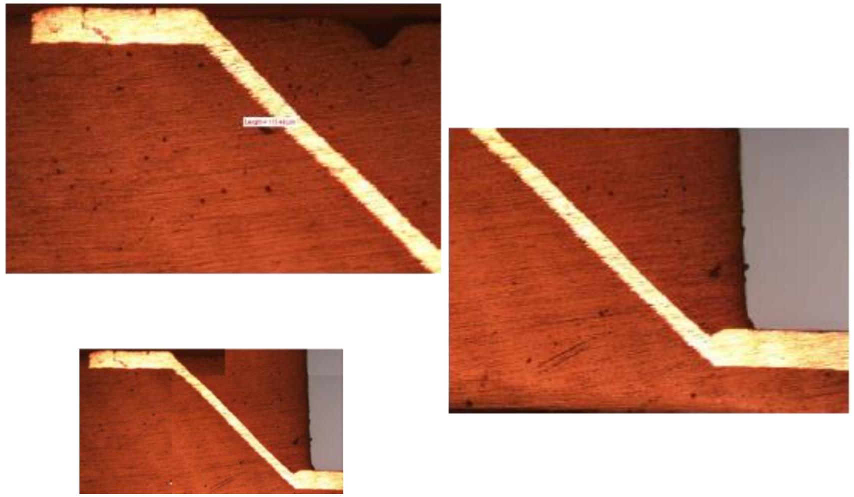
- Homogeneous Z-axis structures allow to 45 degrees vias with increased performance and space reduction

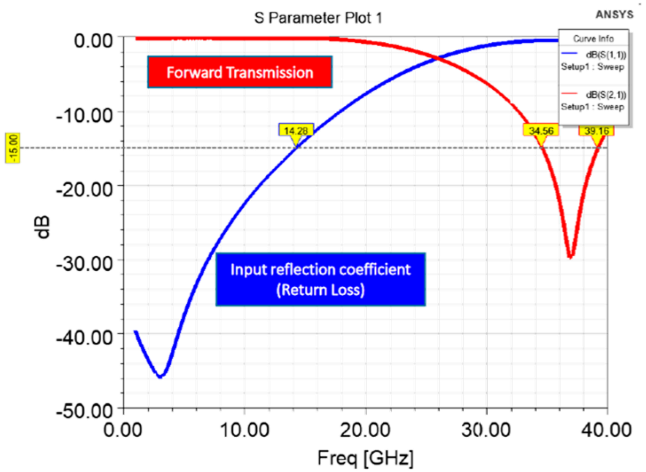
Traditional PCB Process

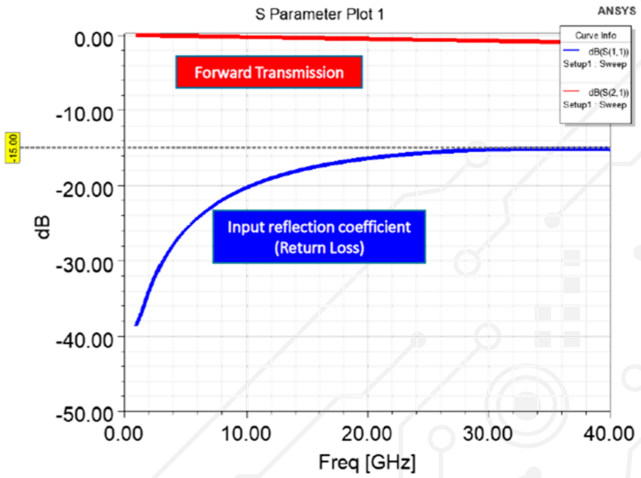


3D AME Process



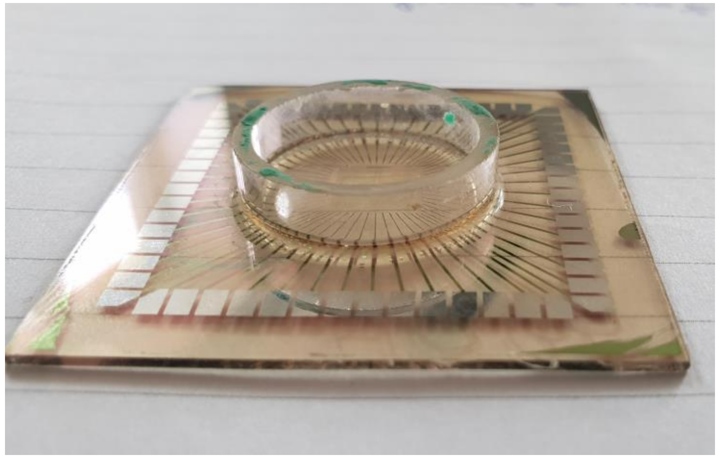


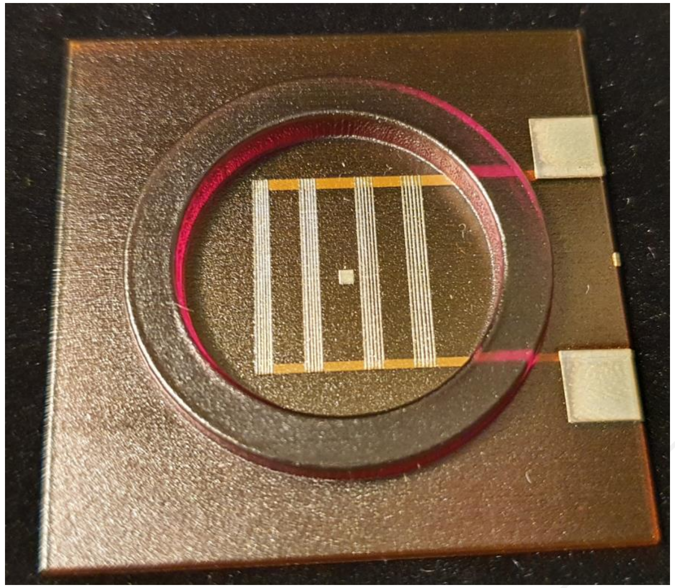




New Design Thinking

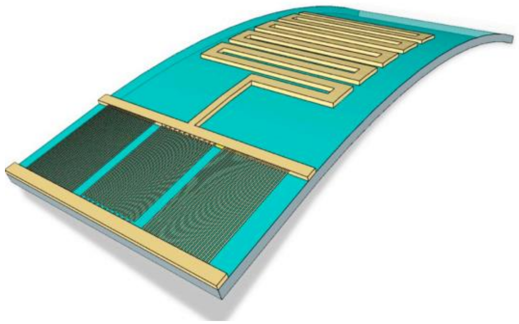
MEDICAL / CELL CULTIVATION



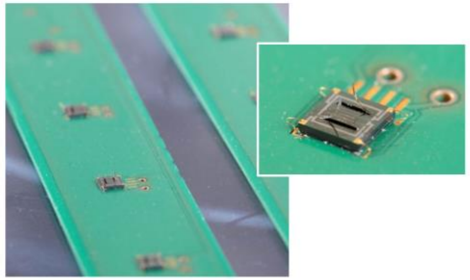


New Design Thinking

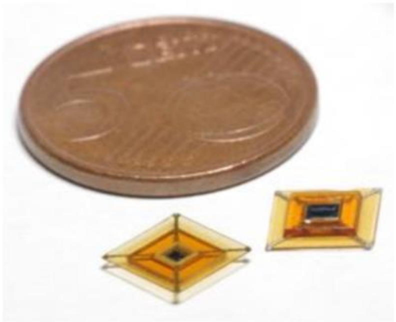
SENSOR APPLICATIONS



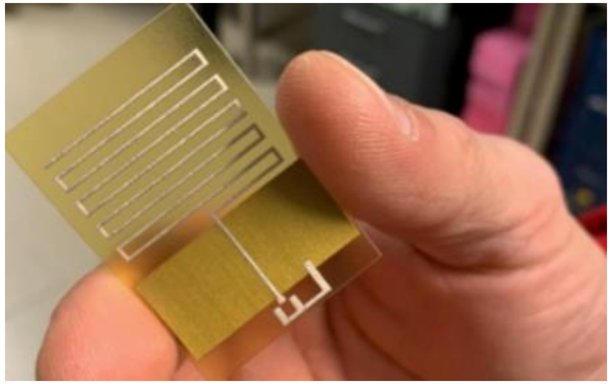
Artificial Hair Cells for Flow Sensing



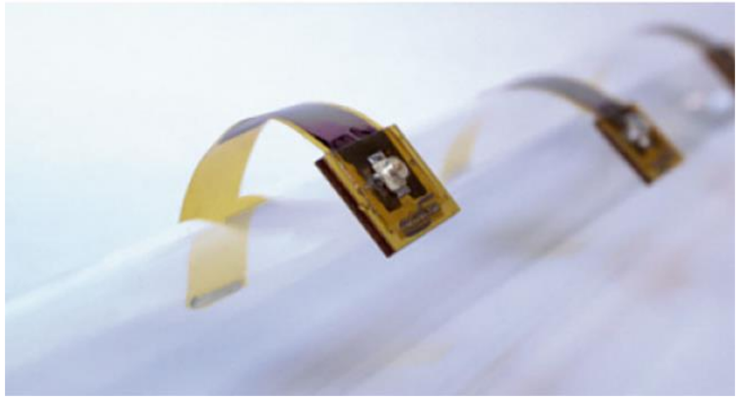
EMBEDDING FLOW SENSORS IN SEALED PACKAGE



Sensor direct print packaging (avoid wirebonding)



Compact and flexible meander antenna for Surface Acoustic Wave sensors



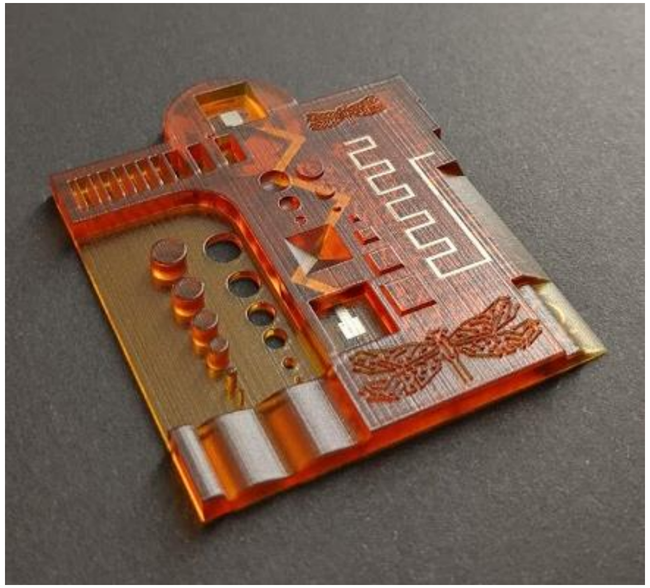
3D embedded sensor in electrical packaging

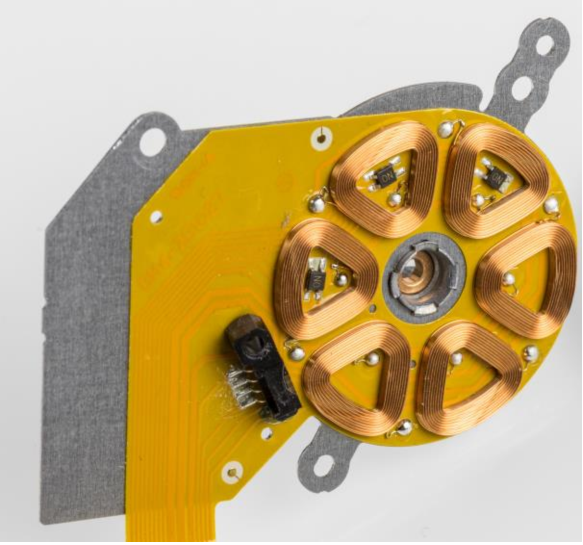
Optoelectronic Neural Surface

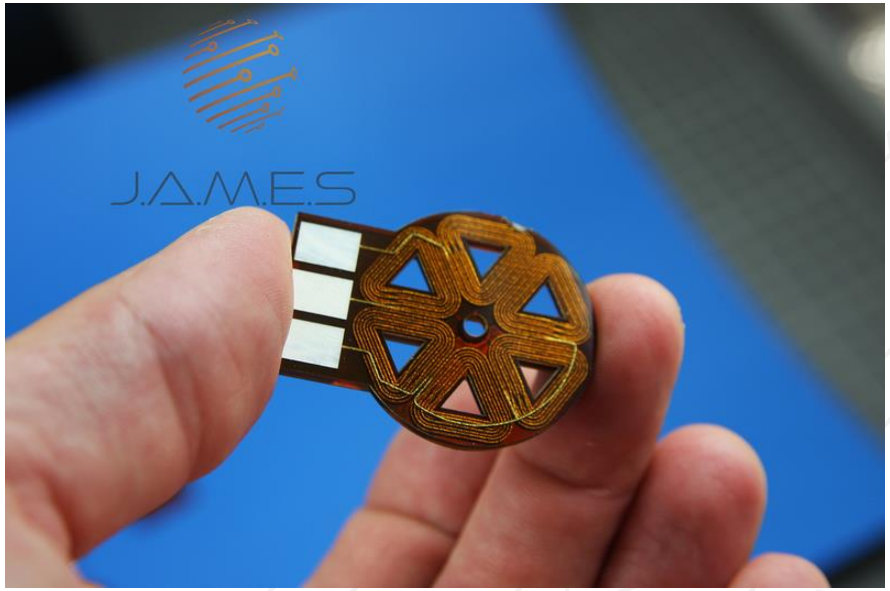
New Design Thinking

ELECTROMECHANICAL

- Multi-step mechanical assemblies can just be printed overnight







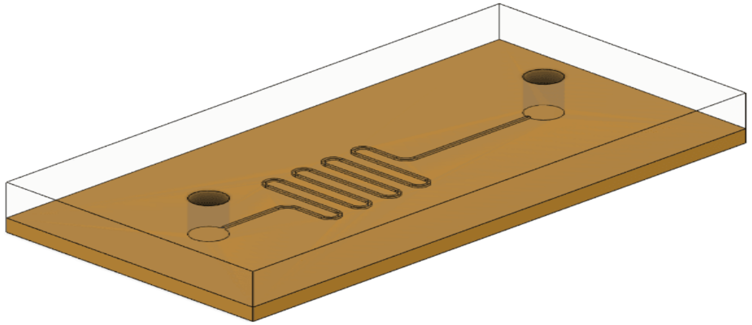
Source: J.A.M.E.S

AME Potential: Applications

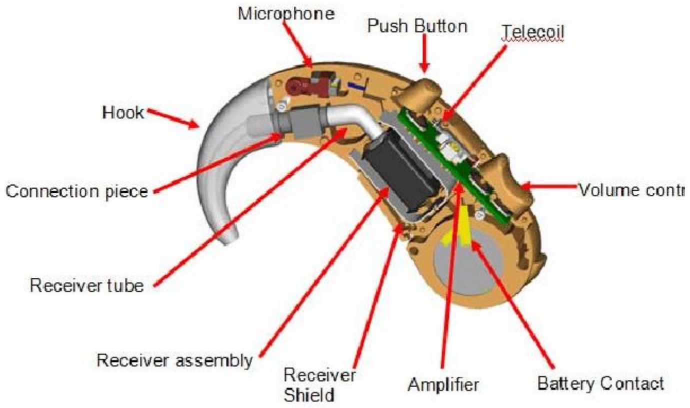
HI PEDS

- High Performance Electronic Devices
  - Composition of several electromechanical techniques in one device

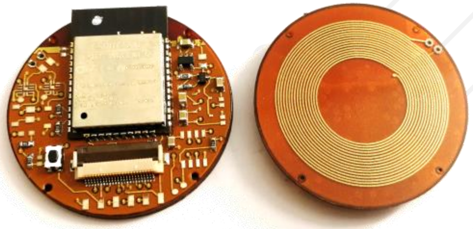
Helical antenna transmitter with holiday theme



Microfluidic Lab-on-chip



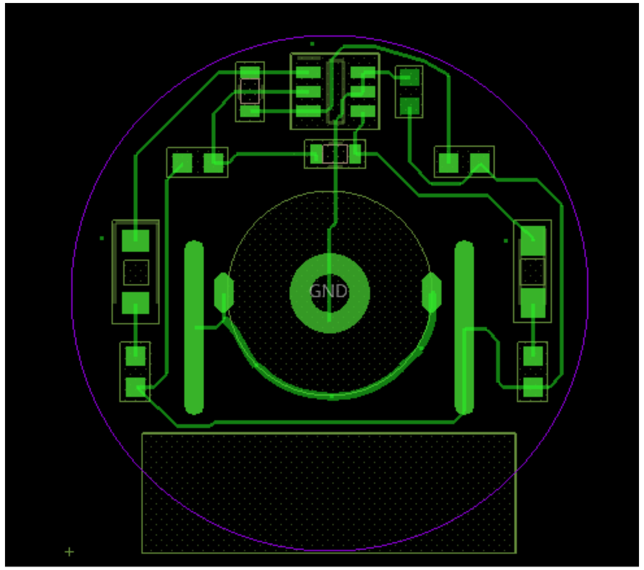
Custom to patient 3D printed hearing aids

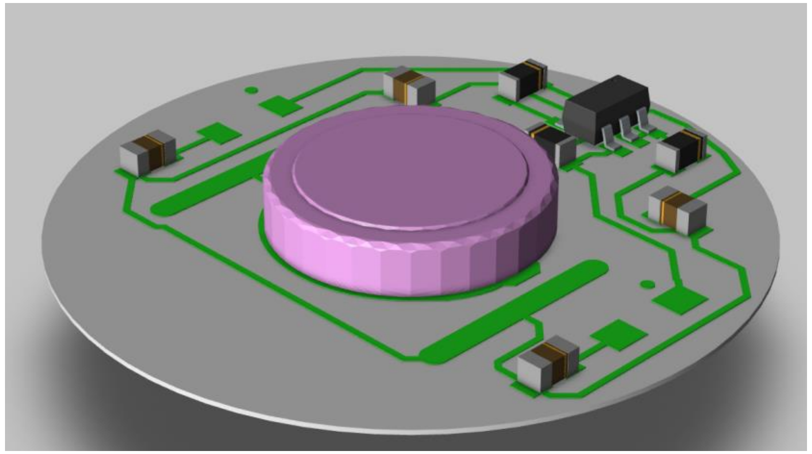
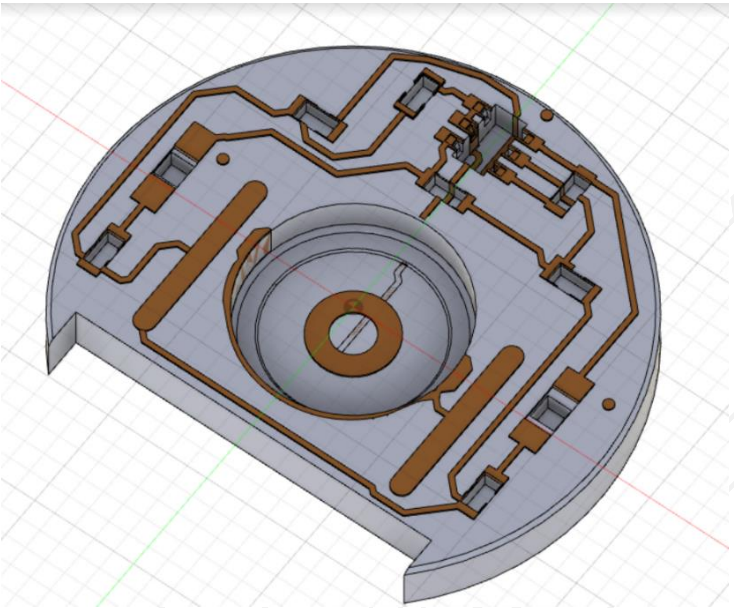


Wireless-powered wireless computing module

Going from 2D to 3D CAD

- Regular 2D ECAD can be converted to 3D ECAD and hence 3D printed.



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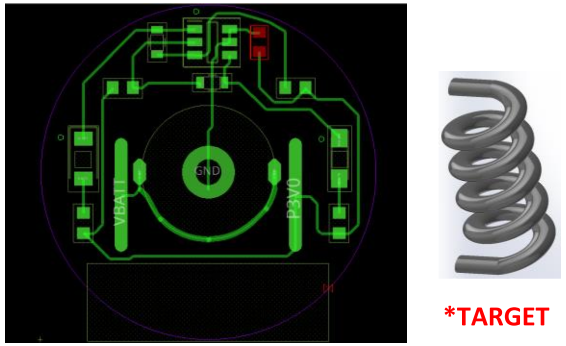
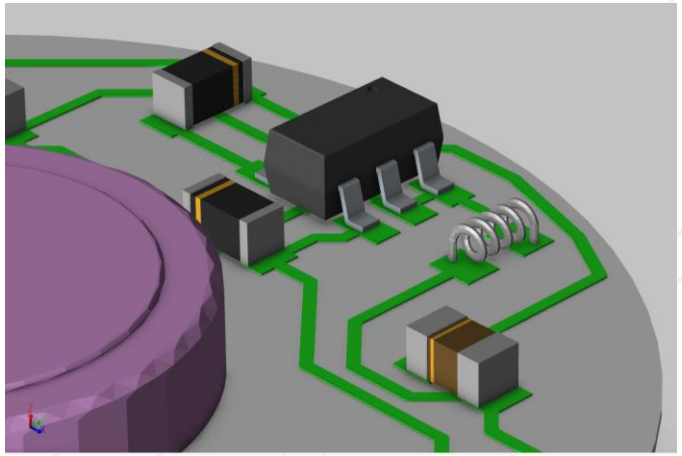
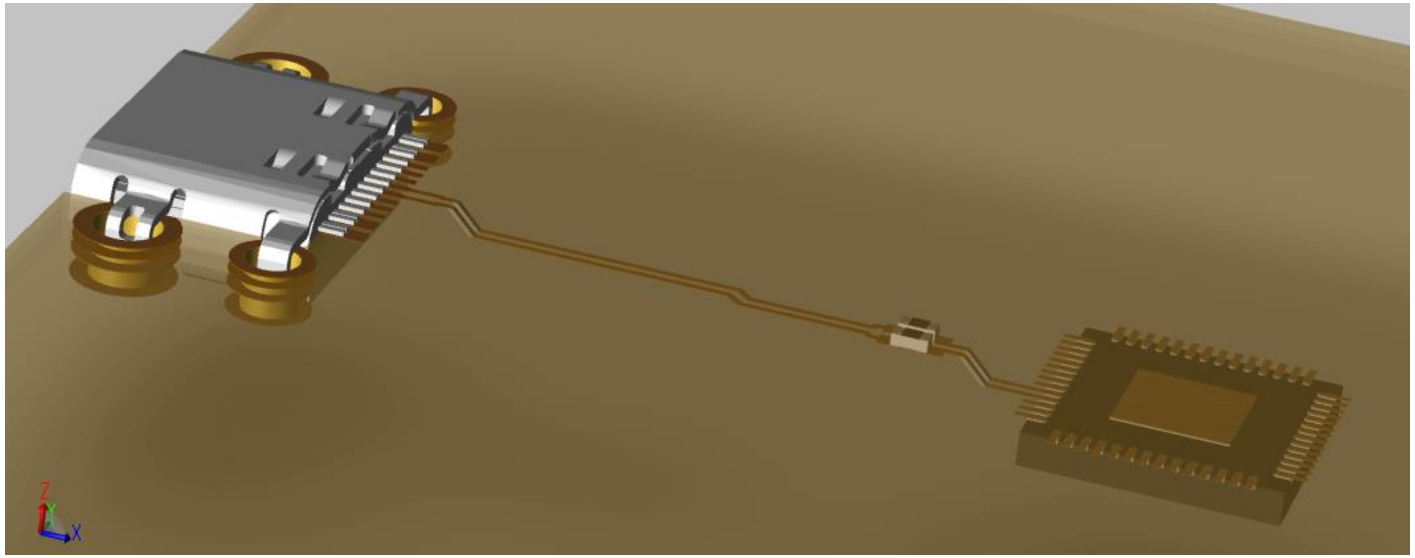


*TARGET



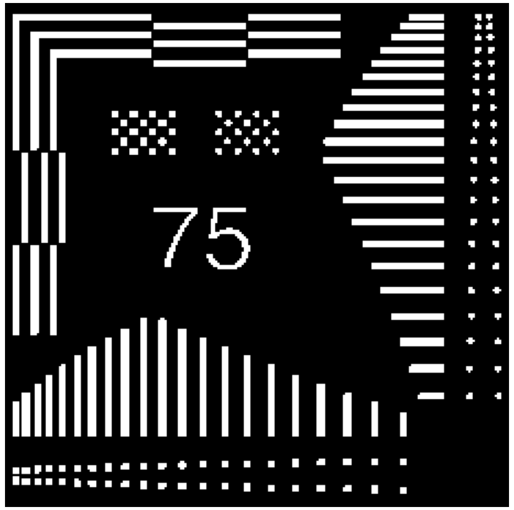


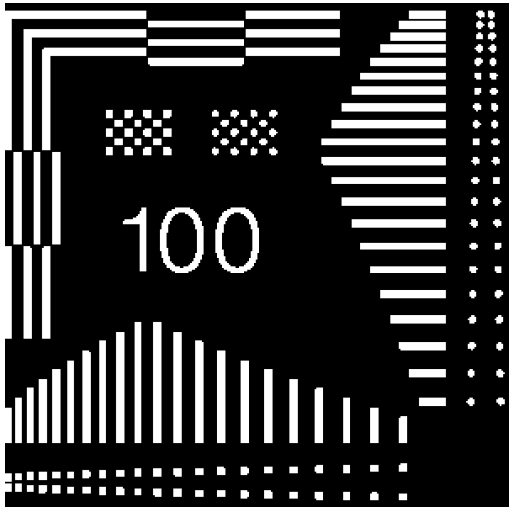
So keep thinking outside of the box

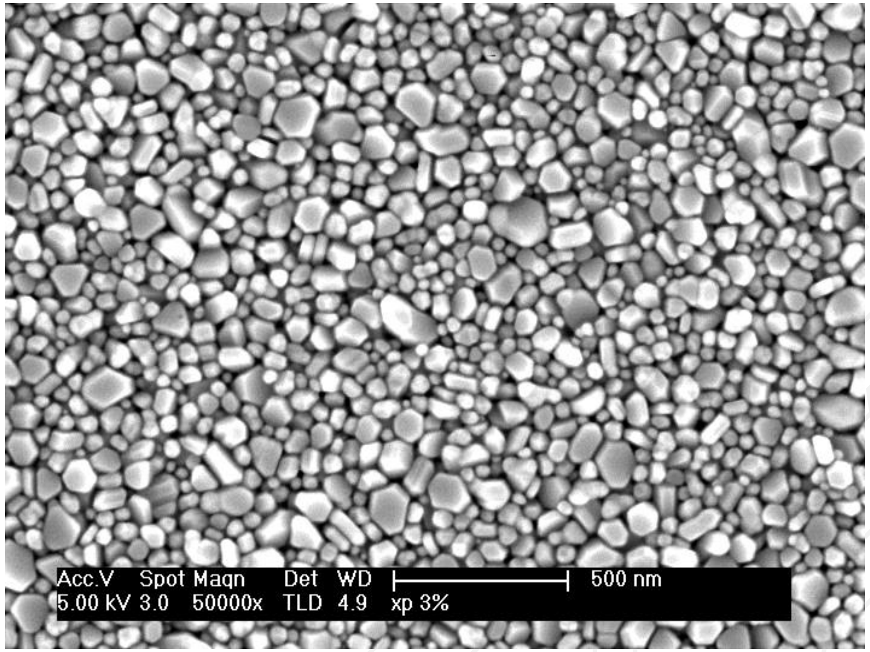
UNLEASH AME POTENTIAL – APPLIED PHYSICS

- Dimensional accuracy, slice over slice.
- AgCite™ Nanoparticle Silver Ink

DragonFly IV & FLIGHT







THANK YOU

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BACKUP

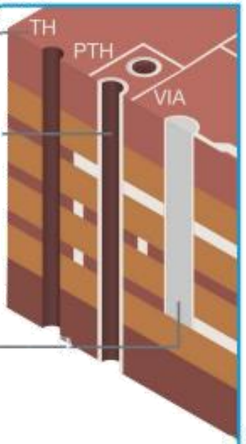
Design Rules

Min Trace Width 75µm ± 9µm

Min Electrical Clearance / Space

Clearance/Space	Trace Thickness
100µm ± 9µm	17µm - 50µm
150µm ± 9µm	50µm - 100µm

Minimum PTH/Via release/clearance: 250µm



Through Hole (TH)
Min: 400µm ± 18µm

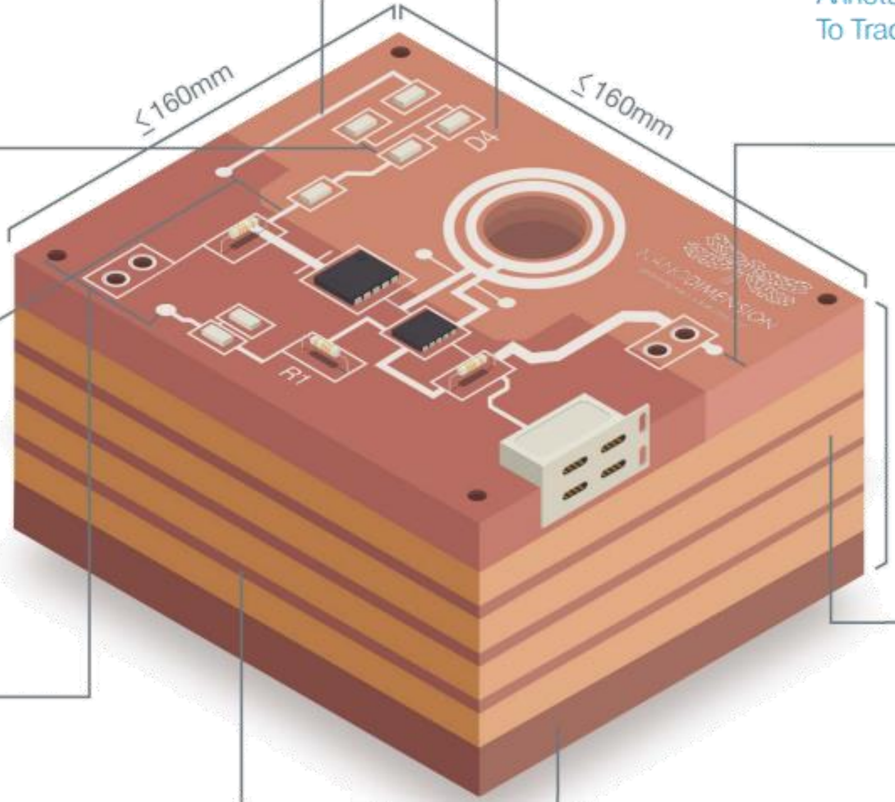
Plated Through Hole (PTH)
Min: 400µm ± 18µm

Pad surrounding PTH ≥ (TH diameter + 150µm plating ring +200µm). Ensures continuity of conductive material.

Via
Min: 150*µm ± 18µm

Pad surrounding via ≥ (via diameter + 200µm). Ensures continuity of conductive material.

*Expected by Q3, 2022. Currently - minimum 200µm



Annotation Clearance To Trace > 180µm

Edge Spacing
0.5mm (When no edge plating)

0.7mm ≤ Thickness ≤ 3mm ±5%

Minimum Prepreg Above Layer

Signal/plane thickness ± 5%	Min Prepreg above layer
17µm	50µm
35µm	75µm
70µm	125µm
100µm	150µm

Signal / Plane Layer Thickness
Min: 17µm, 6µm steps up to 101µm

Top / Bottom Solder Mask Thickness
50µm

Ink properties

	200MHz	500MHz	1GHz	2GHz	5GHz	10GHz	15GHz	20GHz
Dielectric Constant (Dk)	2.92	2.89	2.86	2.77	2.83	2.80	2.78	2.73
Tangential loss (Df)	0.024	0.021	0.023	0.015	0.023	0.017	0.018	0.017

Table 2 - Electrical Dielectric Properties: Dk and Df as Functions of Operational Frequency

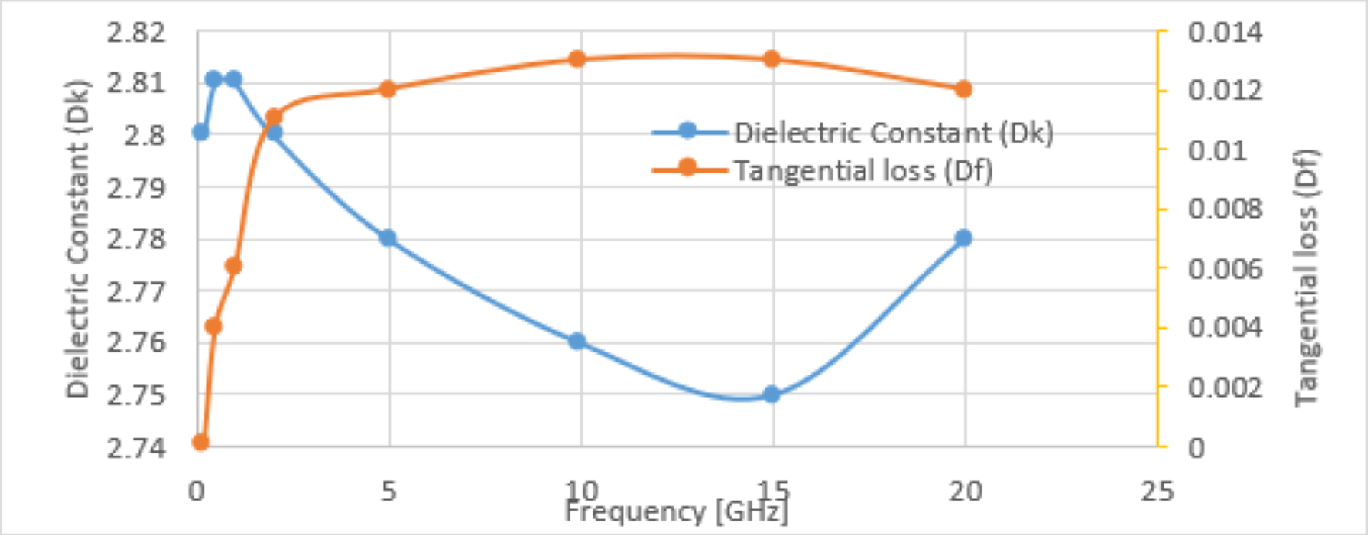


Figure 4: Dk and Df as a function of frequency

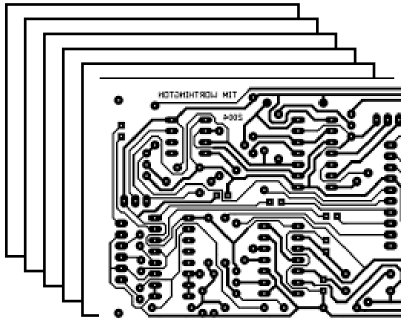
Note: DI electrical parameters, Df and Dk, are a reference. The actual number, especially the Df, is strongly dependent on the test methodology.

Ink properties

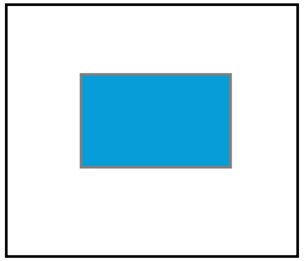
	1092	Test direction	Unit	Condition	Test Method*
Dielectric breakdown (thickness 0.6mm)	40.3		kV		IPC-TM-650 2.5.6
Volume resistivity	3.45e+15		MΩ•c m	After humidity conditioning	IPC 2.5.17.1
	1.53e+14		MΩ•c m	At elevated temperature	IPC 2.5.17.1
Surface resistivity	1.12e+10		MΩ	After humidity conditioning	IPC 2.5.17.1
	1.64e+11		MΩ	At elevated temperature	IPC 2.5.17.1
Arc resistance	TBD		Sec		IPC 2.5.1
Moisture absorption	1.30		%		IPC-TM-650 2.6.2.1
Flexural strength (crosswise)	106.4		N/mm2	23 °C	IPC TM-650 2.4.4
CTE X/Y/Z (TMA) (thickness ≥ 0.5 mm)	108/117/131	X, Y, Z	ppm/°C	35°C-230°C, no pretreatment	IPC-TM-650 2.4.24
	107/104/128	X, Y, Z	ppm/°C	35°C-230°C, pretreatment: 105 °C, 2 h	
Decomposition temp. (Td 2%) (TGA)	302		°C		IPC-TM-650 2.4.24.6
Decomposition temp. (Td 5%) (TGA)	351		°C		
Tg (DMA, 10 Hz, tan delta)	162		°C		IPC-TM-650 2.4.25 (2.4.24.4)
Flammability	TBD		sec		UL 94
Thermal conductivity	0.21899		W/mK	23 °C	ISO 22007-2
Thermal diffusivity	0.13606		mm^2/ sec	23 °C	

DFIV Resolution

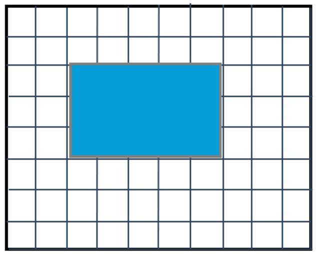
From Vectors to Pixels – Rendering by FLIGHT Control



Gerber / Excellon files
or Slice (subset of STL file)
Represents a
layer



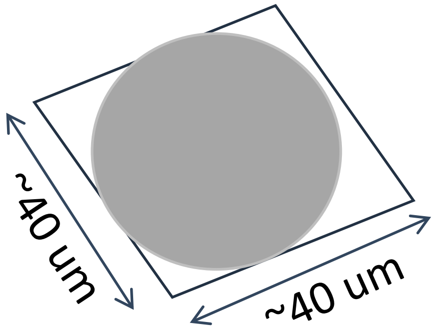
Vector in a
Gerber/Excellon/Slice



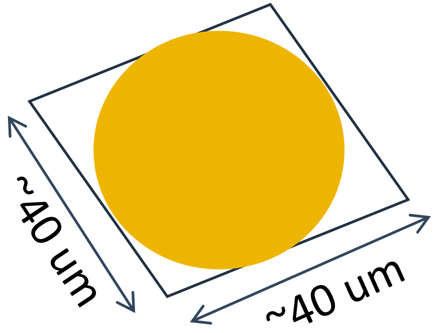
Pixels in a digital file
18umX18um

Drop X,Y Dimensions

Drop X,Y dimensions depend on the **ink material properties**, number of **active print head** nozzles and the **print head voltage** calibration



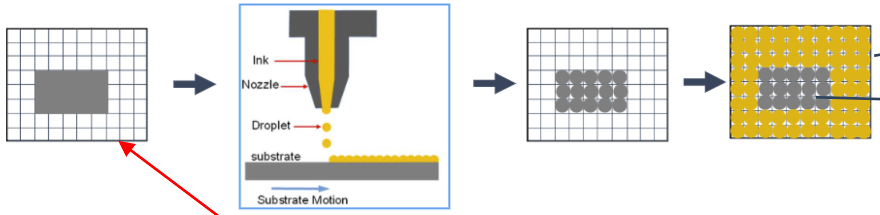
CI

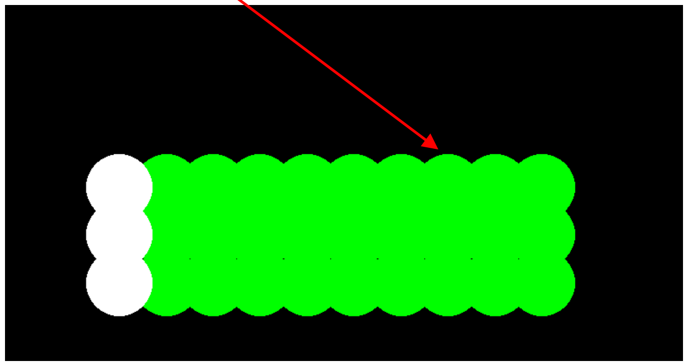


DI

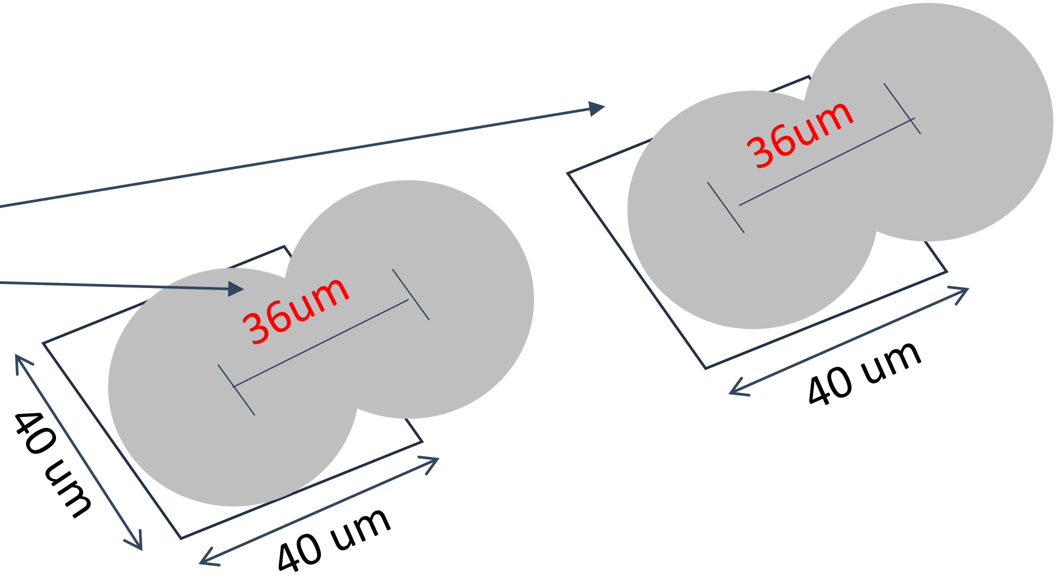
When Print Resolution is 36um (LDM2/LDM/Pro)

Jet every 36 um



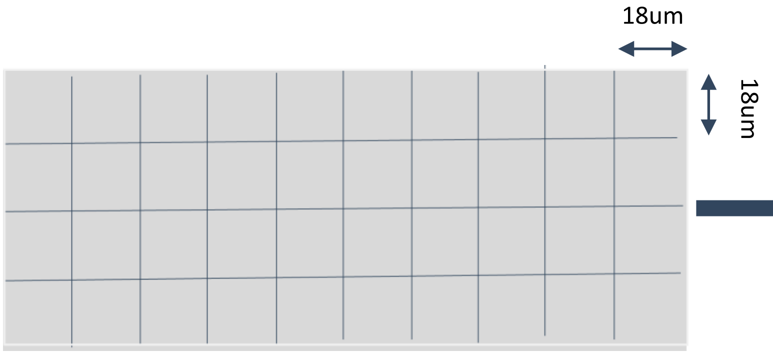


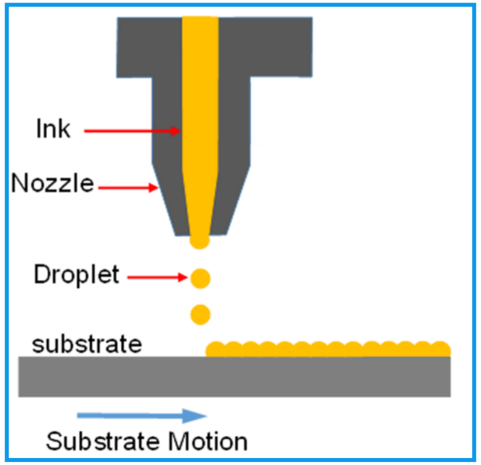
SW

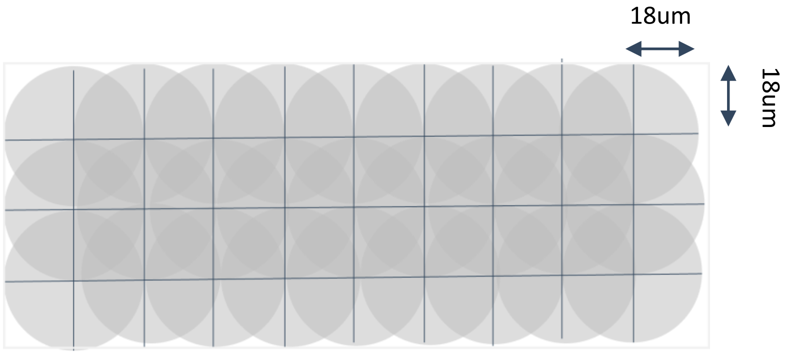


Actual – Edges overlap of drops

When Print Resolution is 18um (DF IV)

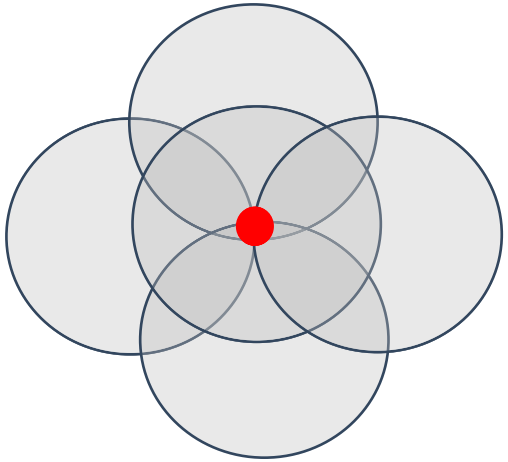


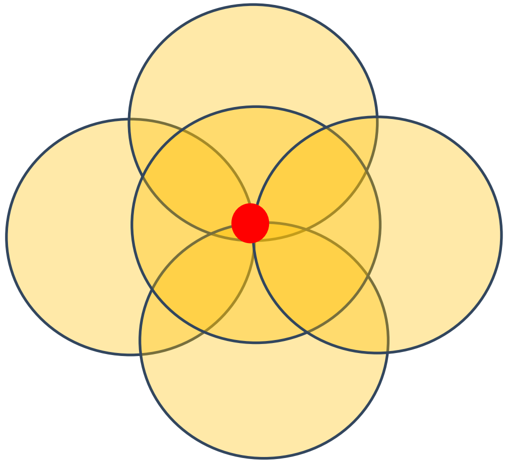




- Pixel - Instruction to the print head to jet a drop
- The distance between jet start is 18um
- Drops overlap - drops size and smearing effect
- Edges of the feature – lower thickness

Pixel = 18um X 18um

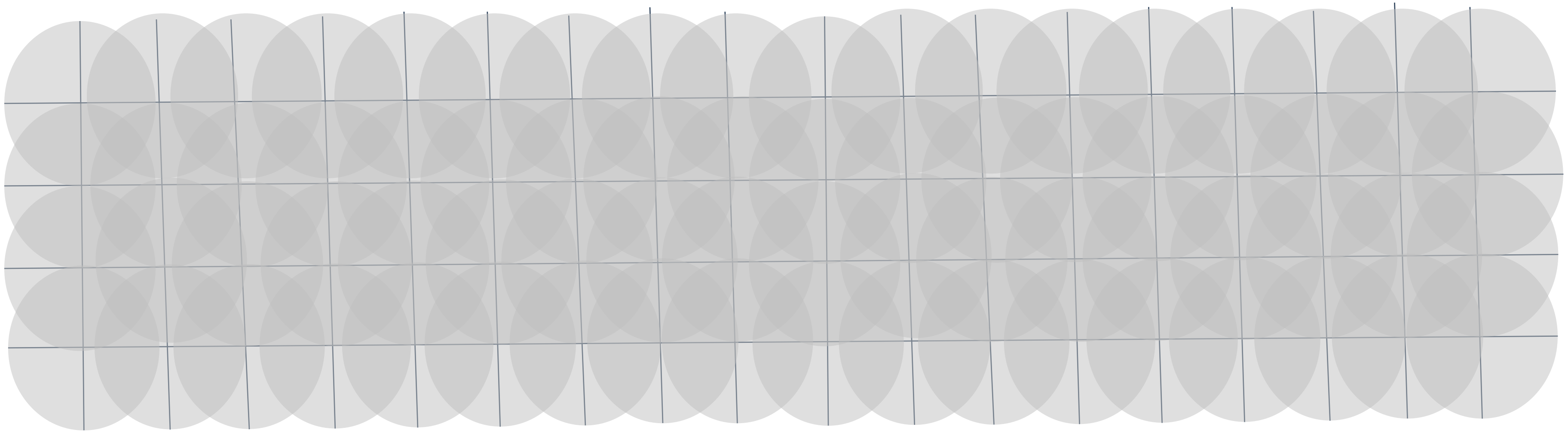




Feature Width Calculation

The algorithm decides how many pixels to set for a trace/feature in a certain width

- Based on research and printer best practice - Drops overlap optimization
- Examples
  - 100um trace width - 4 pixels
  - 75um 2 pixels
- Automatic calculation by FLIGHT Control algorithm (dilation/erosion mechanism)
- Consistency - exact same number of pixels to all traces with the same width in the layer



NANODIMENSION
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Feature Width – By the FLIGHT Control SW

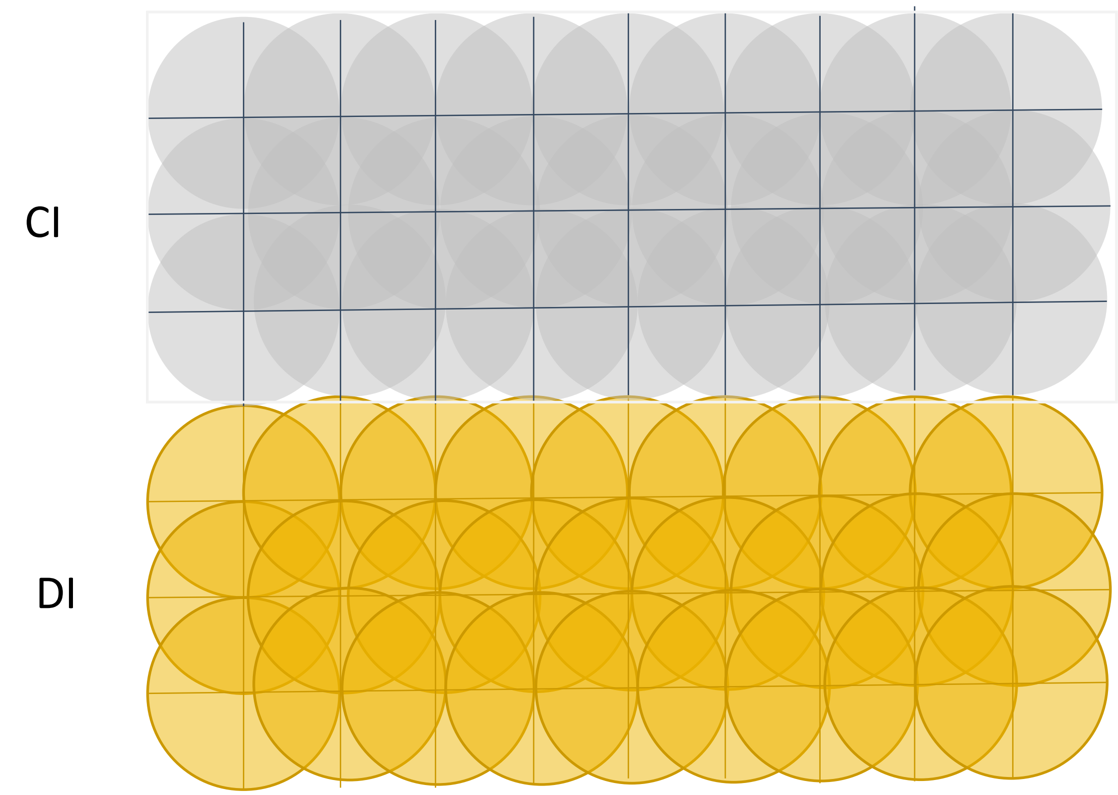
- Conductive features width in FLIGHT Control are rounded to a multiple of 18
- Tolerance of ± 9um between the design width to the SW representation of this feature

Desired Width	Calculation	SW Width
100	100/18=5.55 > 6	108
75	75/18=4.166 > 4	72
98	98/18=5.44 > 5	90

Then:

- FLIGHT Control deducts 2 from the calculated result =(width/18)-2.
- The result is the number of jetted drops
- This compensates on the drop actual XY dimensions (vs. 18 um pixel) including smearing effect

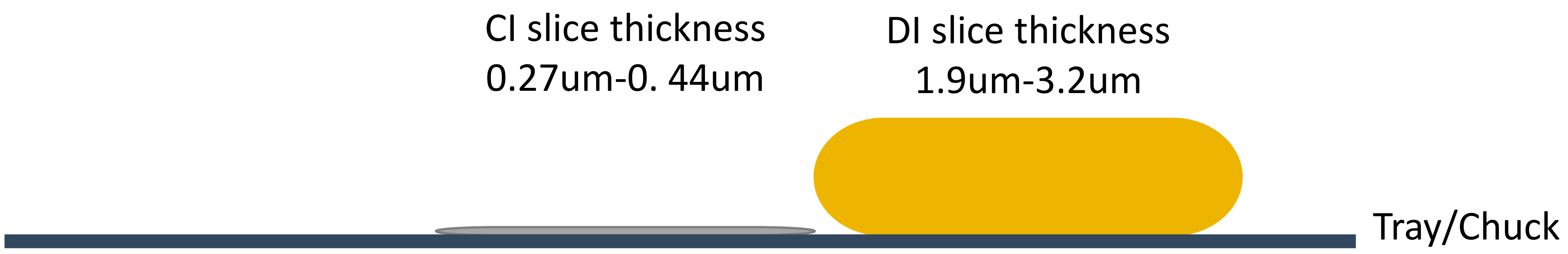
Drops Overlap Ensures Material Continuity



Slices and Layers

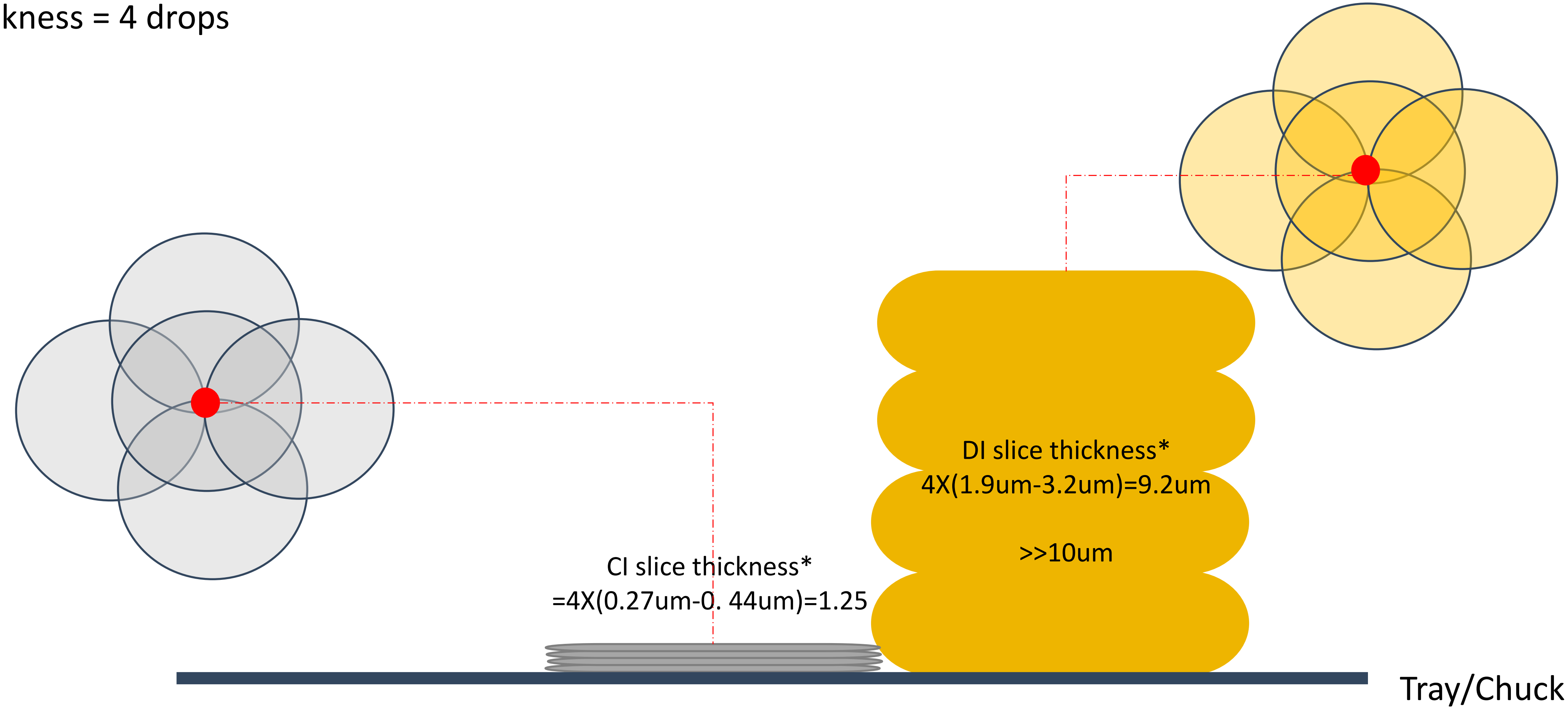
LDM/LDM2 - Slice Thickness 1 drop

- Slice thickness, like droplet thickness is a range affected by ink properties and pphysical factors
- CI Slice – CI drops, thickness is 1 CI drop height
- DI Slice – DI drops, thickness is 1 DI drop height
- Ignore edge overlap for slice thickness calculation



DF IV - Slice Thickness – 4 drops on the z axis

- Slice thickness = 4 drops



*Thickness of 4 drops overlap

CI is Jetted First

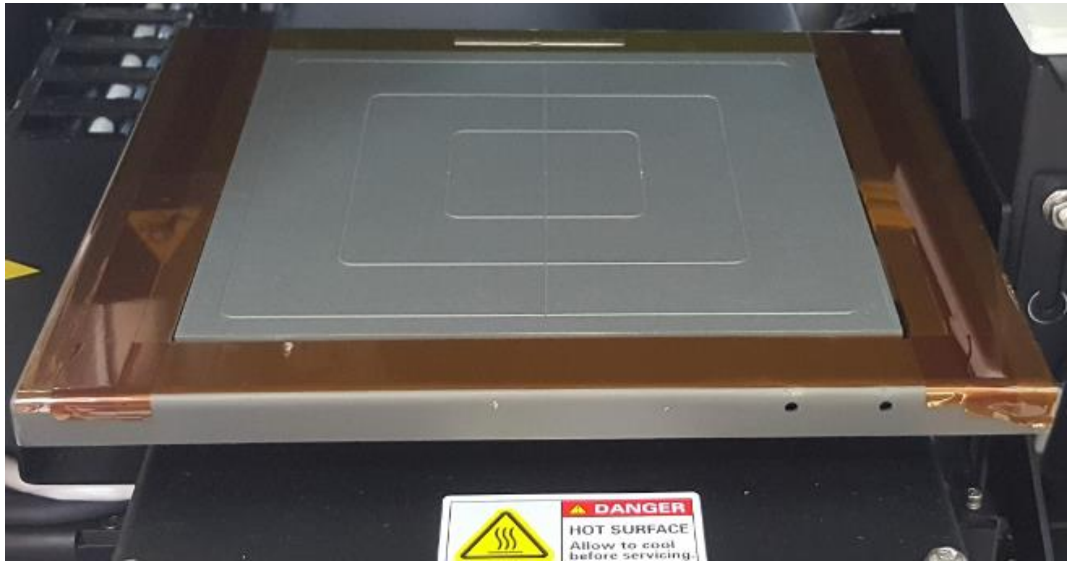
- The CI slices are jetted first to ensure conductivity along the Z axis of the AME slice
- Along the buildup – CI always higher than DI: min 17 um max 35
  - Handle DI tendency to spill over CI
  - And compensate the inaccuracies of slice thickness during the print
- DI is the negative of CI
- Number of CI slices per AME slice is set based on the DI/CI thickness ratio (9-11)
- CI-DI thickness gap is closed in the last slice of the layer (up to 1.25um difference between CI – DI because = Ci slice thickness)

AME Device Dimensions

Maximum AME Dimensions

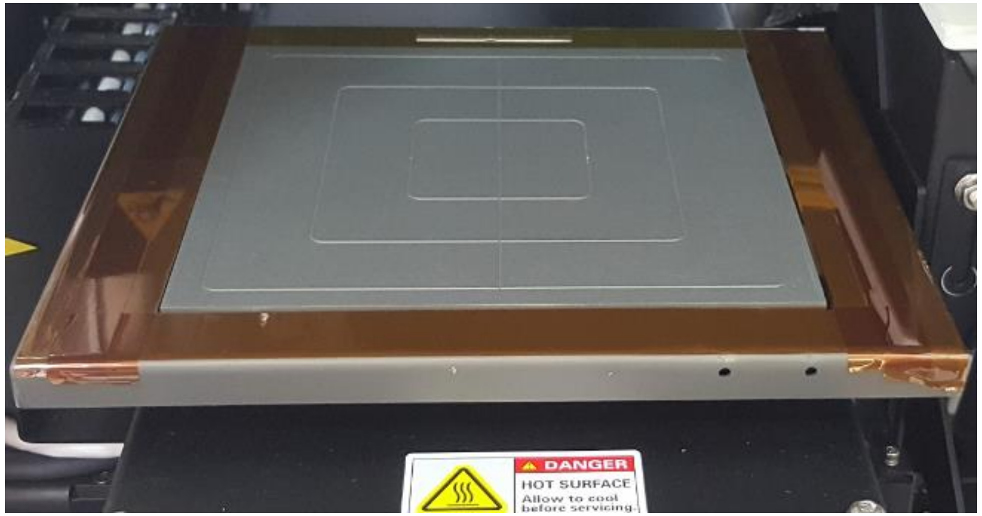
<u>The Rule</u>: 160 x 160 x 3 mm (x, y, z)

6.3 x 6.3 x 0.12 inch



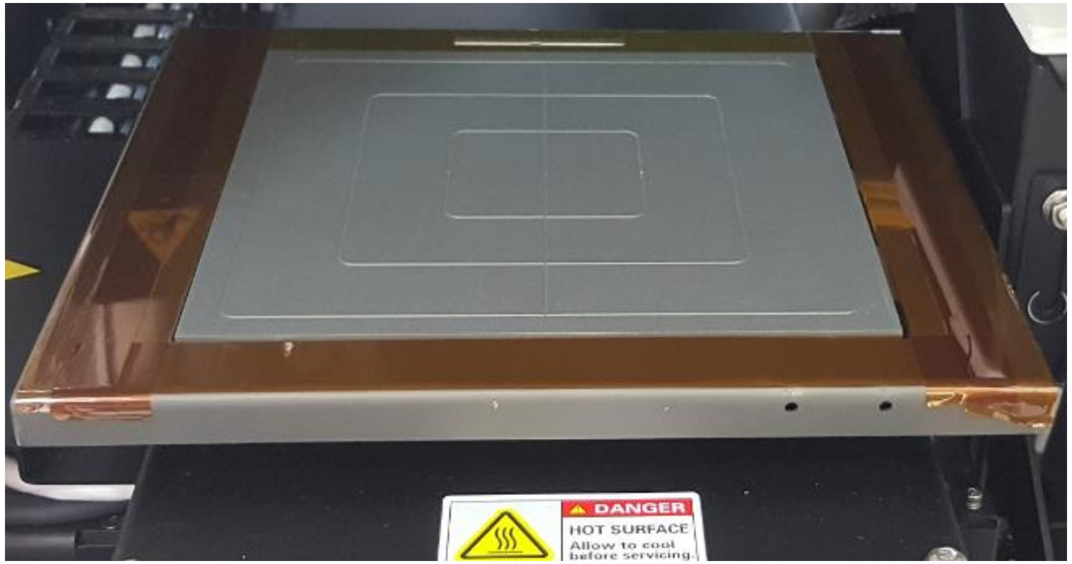
Maximum 160 X 160 MM / 6.3 x 6.3 inch

- Chuck dimensions: 200 mm X 200 mm / 7.87 inch X 7.87 inch
- The edges of the chuck are reserved for calibration printings (e.g. thickness calibration board)
- Preventing edge effect
  - Chuck temperature -160°C. (140°C LDM).
  - Printing too close to the chuck edge will cause an uneven thermal environment around the printed board and will influence materials behavior



Maximum 3 mm / 0.12 inch / 118.11 mil

- As thickness increases the print accuracy is decreased
- Accumulative height error of 5%
- The design rules developed and tested up to 3mm height



 |

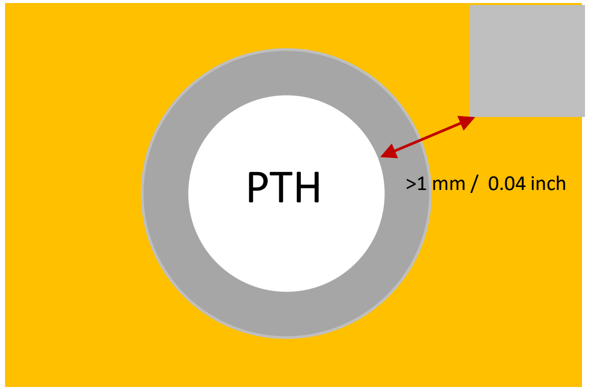
Minimum AME Thickness

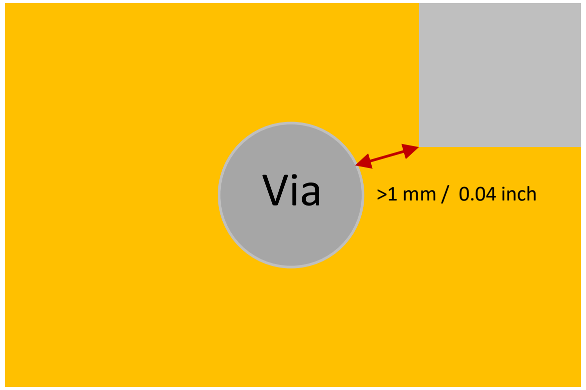
The Rule: Minimum AME thickness is 0.7 mm / 27.56 mil:

- To get a mechanical strength that will allow the board to be disconnected from the substrate without breaking

Signal vs. Plane Layer

- **Signal layer** - A layer of traces that its polygon planes distance from the vias and Plated Through Holes (PTH) is more than 1 mm / 0.04 inch





- **Plane layer** - a conductive polygons layer
- In FLIGHT Control SWITCH®/ software - both the plane and the signal are tagged as a signal

Signal / Plane Layer Thickness Rule

Min: 17 um, up to 100 um, Tolerance 1.5um

Min: ½ oz to 2.9 oz

Min: 0.67 mil to 3.98 mil

Min 17 um / ½ oz / 0.67 mil

- Same as the industry standard
- Tests showed that 17um layers work well
- Less than that is applicable technically but has not been tested

Layer Thickness Up to 100 um / 2.9 oz / 3.98 mil:

Above 100 um / 2.9 oz / 3.98 mil: Not recommended since sintering quality will be reduced

Prepreg Between Signal/Plane Layers

Signal/plane thickness ± 5%	Min prepreg above conductive layer
17-34 µm	50µm
35-69 µm	75µm
70-99 µm	127µm
100 µm	150µm

Minimum Recommended Trace / Clearance Width

Trace & Clearance Rules in the 2D Signal Layer

AME is digitally printed and has pixelization effects. All features apart from the thickness have discrete steps of 18μm squares. All other steps are converted to this scale.

	Value (μm)	**Trace thickness (μm)**
Minimum recommended trace width	75 ± 9	<100
Minimum recommended electrical clearance	100 ± 9	17-50
Minimum recommended electrical clearance	150 ± 9	50-100